NONVOLATILE MEMORY AND METHOD OF MAKING SAME

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Field of the Invention

[0001] The present disclosure relates, in general to memory devices, and more particularly, to a nonvolatile memory device and method of making the same.

Related Art

[0002] It has been shown that non-volatile memory single-transistor bitcells having a dielectric with embedded silicon nanocrystals can be charged with electrons using hot carrier injection (HCI injection), HCI injection with reverse well/source bias, or Fowler-Nordheim (FN) tunneling. The nanocrystals can be discharged with Fowler-Nordheim tunneling through either a top or a bottom dielectric with respect to the nanocrystals. The array architecture considerations of either FN tunneling program/erase or HCI program / FN erase for single-transistor bitcells are also understood. While vertical FN programming is a very low current operation, it results in a long programming time (e.g., on the order of 1-10 msec) and an inefficient bitcell with either two transistors per bitcell or two parallel conductors in a bitline direction. HCI programming results in an efficient bitcell and fast programming (e.g., on the order of 1-10 μsec) at the expense of high programming current (e.g., on the order of 100-200 μA).

[0003] It also has been shown that source-side injection in a split-gate bitcell in combination with an oxide-nitride-oxide (ONO) storage layer can be used with either hot hole erase or with erase through the thin top oxide of a SONOS device. However, hot hole erase results in oxide degradation leading to read disturb, and thin top oxide erase of an ONO layer results in susceptibility to read disturb for erase times on the order of between 100 msec to 1 sec.

[0004] Accordingly, a bitcell combining high reliability program/erase operations and low write power is needed.

Brief Description of the Drawings

[0005] The present invention is illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

[0006] Figure 1 is a cross-sectional view of a nonvolatile memory device having a split gate with nanoclusters embedded within a dielectric layer for charge storage according to one embodiment of the present disclosure;

[0007] Figure 2 is a cross-sectional view of a nonvolatile memory device having a split gate with nanoclusters embedded within a dielectric layer and disposed under polysilicon spacers according to another embodiment of the present disclosure;

[0008] Figure 3 is a schematic diagram of a nonvolatile memory device according to another embodiment of the present disclosure; and

[0009] Figure 4 is a cross-sectional view of a nonvolatile memory device including a shallow implant according to another embodiment of the present disclosure.

[0010] Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present disclosure.

Detailed Description

[0011] Figure 1 is a cross-sectional view of a nonvolatile memory device 10 having a split gate with nanoclusters embedded within a dielectric layer for charge storage according to one embodiment of the present disclosure. Memory device 10 includes a substrate having a bitcell well 12 of a first conductivity type overlying a deep well 14 of a second conductivity type, opposite the first conductivity type. In one embodiment, the first conductivity type includes p-type and the second conductivity type includes n-type dopant.

[0012] Memory device 10 also includes a select gate transistor 15, the select gate transistor including gate dielectric 16 and gate electrode 18. Memory device 10 further includes a control gate transistor 21, the control gate transistor including at least a first dielectric 22, a layer of nanoclusters 24, a second dielectric 26, and a gate electrode 28. In one embodiment, the structure of first dielectric 22, layer of nanoclusters 24, and second

dielectric 26 form a charge storage structure, the nanoclusters being used for charge storage. In addition, the first dielectric 22 includes a top oxide/nanocluster surface and forms an F/N tunneling dielectric. The second dielectric 26 includes a bottom oxide/nanocluster surface and forms the bottom dielectric. In one embodiment, the nanoclusters comprise silicon nanocrystals.

[0013] The select gate transistor 15 is separated from the control gate transistor 21 by a narrow dielectric 20. Narrow dielectric 20 has a dimension on the order of less than 200 angstroms (<20nm) between the select gate and control gate transistors. Narrow dielectric 20 can include, for example, a narrow oxide sidewall dielectric. Memory device 10 also includes source/drain regions 30 and 32. The various layers and doped regions, as discussed herein, of memory device 10 can be fabricated, respectively, using techniques known in the art.

[0014] In one embodiment, the memory device 10 includes a split gate device in which a layer of nanoclusters is embedded between first and second dielectric layers, wherein the split gate device is utilized for non-volatile charge storage. That is, the split gate device has a control gate transistor with nanoclusters embedded between a bottom and top dielectric, and a select gate transistor with a gate dielectric. The first and second dielectric layers include dielectrics having a thickness on the order of 35-70Å. In addition, the transistors of the split gate device are separated by a narrow dielectric area, such that source side injection is possible.

[0015] Examples of source side injection with biases as applied to the 1-bit storage cell of memory device 10 are provided in Table 1 and Table 2. That is, Table 1 provides various bitcell operating voltages for carrying out an erase operation performed with Fowler-Nordheim tunneling through the top dielectric 26 of the 1-bit storage cell of memory device 10. In addition, Table 2 provides various bitcell operating voltages for carrying out an erase operation performed with Fowler-Nordheim tunneling through the bottom dielectric 22 of the 1-bit storage cell of memory device 10. Read current flows in the opposite direction to the write current.

[0016] In the embodiment of Figure 1, the bitcell operating voltages are as follows. Bitcell well 12 of memory device 10 includes a p-type well at a bitcell well voltage, Vpw. Select gate 18 includes a polysilicon select gate, wherein a select gate voltage, Vsg, is applied

to the same. Control gate 28 includes a polysilicon control gate, wherein a control gate voltage, Vcg, is applied to the same. Source and drain regions (30, 32) are at respective source/drain voltages, Vsource/Vdrain. In the tables, Vdd represents a positive supply voltage, b/c Vt represents the bitcell threshold voltage, and "float" represents neither coupled to a voltage or ground.

Table 1: Bitcell operating voltages for erase through top oxide for 1-bit storage.

Terminal	*Source*	*Select Gate*	*Control Gate*	*Drain*	*Bitcell P-Well*	*Deep N-Well*
Programming, selected bitcell	5V	1V	5V	0V	0V	Vdd
Programming, unselected bitcell	5V	0V	0V or 5V	5V	0V	Vdd
Erase, selected sector	-6V or float	-6V or 0V	6V	-6V or float	-6V	0V
Erase, unselected sector	0V or float	0V	0V	0V or float	0V	0V
Read, selected bitcell	0V	Vdd	Vdd or 0V, but > b/c Vt	1V	0V	Vdd
Read, unselected bitcell	0V	0V	Vdd or 0V, but > b/c Vt	0V	0V	Vdd

Table 2: Bitcell operating voltages for erase through bottom oxide for 1-bit storage.

Terminal	*Source*	*Select Gate*	*Control Gate*	*Drain*	*Bitcell P-Well*	*Deep N-Well*
Programming, selected bitcell	5V	1V	5V	0V	0V	Vdd
Programming, unselected bitcell	5V	0V	0V or 5V	5V	0V	Vdd
Erase, selected sector	6V or float	0V	-6V	6V or float	6V	6V
Erase, unselected sector	0V or float	0V	0V	0V or float	0V	0V
Read, selected bitcell	0V	Vdd	Vdd or 0V, but > b/c Vt	1V	0V	Vdd
Read, unselected bitcell	0V	0V	Vdd or 0V, but > b/c Vt	0V	0V	Vdd

[0017] Figure 2 is a cross-sectional view of a nonvolatile memory device 40 having a split gate with nanoclusters embedded within a dielectric layer and disposed under polysilicon spacers according to another embodiment of the present disclosure. In the embodiment of Figure 2, the device 40 is built with control gates 52 formed by poly spacers. Accordingly, two bits can be stored, one bit on either side of the select gate 44.

[0018] In one embodiment, a write operation for the device 40 of Figure 2 has a low programming current on the order of approximately 1-10 μA and a fast programming time on the order of approximately 1-10 μsec. The erase operation operates on a block of bitcells with low erase current and an erase time on the order of approximately 10-100 msec. In typical non-volatile memory devices, the select gate uses a thin gate oxide on the order of approximately 50-100 Å oxide, wherein the thin gate oxide is similar to a low voltage transistor oxide. However, in device 40 of the present disclosure, the select gate 44 includes a high voltage oxide with a thickness on the order of approximately 70-90 Å. Such a high voltage oxide is similar to an input/output transistor (I/O) oxide. The 90 Å-thick oxide is necessary if the bitcell well 12 is biased at +6V or -6V to enable splitting the erase voltages between the bitcell well 12 and a corresponding control gate.

[0019] In another embodiment, the device 40 includes a nanocluster-based memory device having select gate transistor 58; a thin film storage stack consisting of a bottom oxide 46 having a thickness on the order of 50-70 Å, a layer of nanoclusters 48 on the order of 20-25% surface coverage, and a top oxide 50 of a high temperature oxide (HTO) having a thickness on the order of approximately 50 Å; and sidewall spacer control gates 52 on both sides of the select gate 44, over the thin film storage (TFS) stack. Top oxide 50 includes HTO since HTO is a deposited oxide and minimizes the number of electron or hole trap sites in the deposited oxide, as compared with a large number of electron or hole trap sites in a low temperature oxide (e.g., TEOS). Accordingly, the thin film storage stack includes top oxide 50, nanoclusters 48, and bottom oxide 46 in the region disposed below a respective gate electrode 52. In addition, memory device 40 is configured for source-side injection programming and for Fowler-Nordheim tunneling erase through the top oxide 50. The various layers and doped regions, as discussed herein, of memory device 40 can be fabricated, respectively, using techniques known in the art.

[0020] Examples of source side injection with biases as applied to the 2-bit storage cell of memory device 40 are provided in Table 3 and Table 4. That is, table 3 provides various bitcell operating voltages for carrying out an erase operation performed with Fowler-Nordheim tunneling through the top dielectric 50 of the 2-bit storage cell of memory device 40. In addition, table 4 provides various bitcell operating voltages for carrying out an erase operation performed with Fowler-Nordheim tunneling through the bottom dielectric 46 of the 2-bit storage cell of memory device 40. Read current flows in the opposite direction to the write current.

[0021] In the embodiment of Figure 2, the bitcell operating voltages are as follows. Bitcell well 12 of memory device 10 includes a p-type well at a bitcell well voltage, Vpw. Select gate 44 includes a polysilicon select gate, wherein a select gate voltage, Vsg, is applied to the same. Control gates 52 include polysilicon control gates, wherein a first and second control gate voltage, Vcg1, Vcg2, is applied to the same, respectively. Source and drain regions (30, 32) are at respective source/drain voltages, Vsource/Vdrain. In the tables, Vdd represents a positive supply voltage, b/c Vt represents the bitcell threshold voltage, Vo represent a programmed threshold voltage in which the nanocrystals are charged with one or more electrons, and "float" represents neither coupled to a voltage or ground.

Table 3: Bitcell operating voltages for erase through top oxide for 2-bit storage.

Terminal	*Source*	*Select Gate*	*Control Gate 1*	*Control Gate 2*	*Drain*	*Bitcell P-Well*	*Deep N-Well*
Programming, selected bitcell, left bit	5V	1V	5V	5V or 0V	0V	0V	Vdd
Programming, selected bitcell, right bit	0V	1V	5V or 0V	5V	5V	0V	Vdd
Programming, unselected bitcell	5V	0V	0V or 5V	0V or 5V	5V	0V	Vdd
Erase, selected sector	-6V or float	-6V or 0V	6V	6V	-6V or float	-6V	0V
Erase, unselected sector	0V or float	0V	0V	0V	0V or float	0V	0V
Read, selected bitcell	0V	Vdd	Vdd or 0V, but > b/c Vt	(Vdd + Vo) or Vo	1V	0V	Vdd
Read, unselected bitcell	0V	0V	(Vdd + Vo) or Vo	Vdd or 0V, but > b/c Vt	0V	0V	Vdd

Table 4: Bitcell operating voltages for erase through bottom oxide for 2-bit storage.

Terminal	*Source*	*Select Gate*	*Control Gate 1*	*Control Gate 2*	*Drain*	*Bitcell P-Well*	*Deep N-Well*
Programming, selected bitcell, left bit	5V	1V	5V	5V or 0V	0V	0V	Vdd
Programming, selected bitcell, right bit	0V	1V	5V or 0V	5V	5V	0V	Vdd
Programming, unselected bitcell	5V	0V	0V or 5V	0V or 5V	5V	0V	Vdd
Erase, selected sector	6V or float	0V	-6V	-6V	6V or float	6V	6V
Erase, unselected sector	0V or float	0V	0V	0V	0V or float	0V	0V
Read, selected bitcell, left bit	0V	Vdd	Vdd or 0V, but > b/c Vt	(Vdd + Vo) or Vo	1V	0V	Vdd
Read, selected bitcell, right bit	0V	Vdd	(Vdd + Vo) or Vo	Vdd or 0V, but > b/c Vt	1V	0V	Vdd
Read, unselected bitcell	0V	0V	Vdd or 0V, but > b/c Vt	Vdd or 0V, but > b/c Vt	0V	0V	Vdd

[0022] Figure 3 is a schematic diagram of a nonvolatile memory device 70 according to another embodiment of the present disclosure. Memory device 70 includes an array of bit cells arranged in rows and columns, including bit cells according to the various embodiments disclosed herein, indicated by reference numerals 72, 74, 76, and 78, for example. Memory device 70 further includes a row decoder 80, column decoder 82, sense amplifiers 84, and control circuit 88 for controlling row decoder 80 and column decoder 82. Row decoder 80 receives address information via address input 90. Column decoder 82 receives address information via address input 92. Sense amplifiers receive signal information from column decoder 82 and output the amplified information or data out on data output 94. Row decoder 80 decodes address information received on address input 90 and outputs information on appropriate word lines 96, 98. Column decoder 82 decodes address information received on address input 92 and receives information via bit lines 100, 102, 104.

[0023] In one embodiment, the bit cell 72 includes a memory device having a select gate transistor 112 and sidewall transistors 114, 116 disposed on opposite sides of gate transistor 112. Sidewall transistors 114 and 116 include dielectric nanocluster thin film storage memory stacks 118 and 120, respectively. The dielectric nanocluster thin film storage memory stacks 118 and 120 comprise stacks similar to those of Figures 1, 2 or 4. Bit cell 72 further includes source/drain regions 122 and 124 coupled to corresponding bit lines 102 and 104, respectively. Still further, bit cell 72 includes a deep well region coupled to a voltage potential V_{WELL}, as indicated by reference numeral 126.

[0024] Figure 4 is a cross-sectional view of a nonvolatile memory device 130 including shallow implants (132, 134) according to another embodiment of the present disclosure. No assumptions have been made for the charge-neutral control gate threshold voltage of the spacer device of control gate transistors (54, 56). Using shallow antimony or arsenic implants (132, 134) performed after select gate formation (44), the threshold voltage Vt of a respective spacer device can be below zero volts (0 V), thereby alleviating the need for biasing the control gates during a read operation. In other words, the memory device 40 is fabricated with a selectively lower channel doping under a respective spacer device using self-aligned counter doped implants of arsenic (As) or antimony (Sb). Counter dopants of As and Sb are selected due to their ability to not substantially diffuse in subsequent processing steps. In addition, the spacer devices have a channel region on the order of approximately 200-1000 angstroms, i.e., short channel device. Accordingly, the threshold voltage of the spacer devices is lowered without degradation of performance characteristics of the short channel spacer devices.

[0025] Although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed.

[0026] In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

[0027] Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.